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(54) SEMICONDUCTOR DEVICE AND DISPLAY DEVICE MODULE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a liquid crystal display device capable of being stably compatible with high definition of a liquid crystal display.

SOLUTION: A shift register circuit 22 is arranged, which transfers a start pulse signal SP by synchronizing it with a clock signal CK. An input latch circuit 21 is arranged, which fetches display data DR, DG, DB by synchronizing them with the clock signal CK. A sampling memory circuit 23 is arranged, which samples and stores the display data DR, DG, DB based on the transferred start pulse signal SP. The input latch circuit 21 fetches the display data DR, DG, DB in synchronism with both rising and falling of the clock signal CK.

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CLAIMS

[Claim(s)]

[Claim 1] In the semiconductor device which drives an indicating equipment based on

an indicative-data signal A transfer means to transmit the start pulse signal based on a clock signal, A latch means to incorporate the inputted indicative-data signal synchronizing with a clock signal, and to output as synchronous data, Based on the start pulse signal transmitted, it has a sampling means to sample and output the above-mentioned synchronous data. The above-mentioned latch means The semiconductor device characterized by synchronizing and incorporating the above-mentioned indicative-data signal to both the timing of the standup of the above-mentioned clock signal, and falling.

[Claim 2] Said latch means is a semiconductor device according to claim 1 characterized by having the latch circuit of a two-piece unit for carrying out serial-parallel conversion of the indicative-data signal inputted serially.

[Claim 3] Said latch means is a semiconductor device according to claim 1 or 2 characterized by being what carries out serial-parallel conversion of the indicative-data signal inputted serially to both the timing of the standup of the plane 1 of said clock signal, and falling.

[Claim 4] In the semiconductor device which drives an indicating equipment based on an indicative-data signal A transfer means to transmit the start pulse signal based on a clock signal, A latch means to incorporate the inputted indicative-data signal synchronizing with a clock signal, and to output as synchronous data, Based on the start pulse signal transmitted, it has a sampling means to sample and output the above-mentioned synchronous data. The above-mentioned latch means The semiconductor device characterized by synchronizing and incorporating the above-mentioned indicative-data signal to both the timing of each standup of two or more clock signals of each, with which phases differ mutually, and falling.

[Claim 5] Said latch means is a semiconductor device according to claim 4 characterized by having the latch circuit of a four-piece unit for carrying out serial-parallel conversion of the indicative-data signal inputted serially.

[Claim 6] Two or more aforementioned clock signals of each are semiconductor devices according to claim 4 with which the number of each above-mentioned clock signals is characterized by being set up at the time of m (m being two or more integers) so that it may have the phase contrast of $1/(2m)$ mutually.

[Claim 7] Said display is a semiconductor device given in claim 1 thru/or any of 6 they are. [which is characterized by being a liquid crystal display]

[Claim 8] The indicating-equipment module characterized by having a semiconductor device given in any [claim 1 thru/or] of 7 they are.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention drives a display with the indicative-data signal by which digital to analog was carried out, and relates to the display module which has a semiconductor device for indicating by gradation in the above-mentioned display, and it.

[0002]

[Description of the Prior Art] Conventionally, as shown in drawing 11 , the liquid crystal display of the TFT (thin film transistor) method which is the example of representation of an active matrix is known. This liquid crystal display is equipped with the liquid crystal panel 901 and liquid crystal driving gear of a TFT method as the liquid crystal display section, and has the liquid crystal display component which is not illustrated in a liquid crystal panel 901, and the counterelectrode (common electrode) 906.

[0003] the above-mentioned liquid crystal driving gear -- respectively -- IC (Integrated Circuit) from -- it has the becoming source driver 902 and gate driver 903, the controller 904, and the liquid crystal drive power source 905. A controller 904 outputs a control signal S12 to a gate driver 903 while outputting indicative-data D and a control signal S11 to the source driver 902.

[0004] As the above-mentioned control signal S11, there is a Vertical Synchronizing

signal as a Horizontal Synchronizing signal, a clock signal, and a control signal S12. And while each liquid crystal driver voltage output terminal of the source driver 902 is connected to the corresponding source signal line in a liquid crystal panel 901, each liquid crystal driver voltage output terminal of a gate driver 903 is connected to corresponding gate signal Rhine in a liquid crystal panel 901.

[0005] Moreover, the liquid crystal drive power source 905 outputs the various driver voltages impressed to the power source which drives a liquid crystal driving gear (the source driver 902, gate driver 903), or a liquid crystal panel 901.

[0006] The digital display data D inputted serially are inputted into the source driver 902 as the above-mentioned indicative-data D through a controller 904 from the outside. The source driver 902 latches inputted indicative-data D inside in time sharing, carries out serial-parallel conversion and performs digital to analog (it is called a DA translation) after that synchronizing with the above-mentioned Horizontal Synchronizing signal inputted from a controller 904.

[0007] And the analog voltage for a gradation display (gradation display electrical potential difference) obtained by the DA translation is outputted to the liquid crystal display component in a liquid crystal panel 901 corresponding to the liquid crystal driver voltage output terminal (not shown) through the above-mentioned source signal line from a liquid crystal driver voltage output terminal, respectively.

[0008] An example of the circuit block diagram of the above-mentioned source driver 902 is shown in drawing 12 . The source driver 902 consists of a shift register circuit 1302, the input latch circuit 1301, the sampling memory circuit 1303, the hold memory circuit 1304, the level-shifter circuit 1305, a DA translation circuit 1306, an output circuit 1307, and a reference voltage generating circuit 1309 fundamentally.

[0009] First, the start pulse signal SP which synchronized the shift register circuit 1302 with the Horizontal Synchronizing signal is inputted, after that, a synchronization is taken to clock signal CK and the start pulse signal SP is transmitted to n steps of shift register circuits 1302.

[0010] And the n-th step of output of a shift register circuit 1302 is outputted as an output signal SPO, it is inputted as a start pulse signal SP of the source driver 902 of the next step of the source driver 902 by which cascade connection is carried out, and the start pulse signal SP is transmitted similarly hereafter.

[0011] Indicative-data D is compared, respectively, consists of indicative-data DR (red) of 6 bit of **, indicative-data DG (green), and an indicative data DB (blue), and is inputted into the input latch circuit 1301. And after being temporarily latched to the input latch circuit 1301, it is sent to the sampling memory circuit 1303 by clock signal

CK. The sampling memory circuit 1303 samples and memorizes indicative-data D sent to time sharing with the output signal (signal which the start pulse signal SP shifted) of each stage of the shift register circuit 1302 of point **.

[0012] Then, indicative-data D is latched by the latch signal LS based on a Horizontal Synchronizing signal, when it is inputted into the following hold memory circuit 1304 and the data of 1 level period of this indicative-data D are inputted into the hold memory circuit 1304. And during 1 level period, previous indicative-data D is held and is outputted from the hold memory circuit 1304 until the following latch signal LS is inputted that is,.

[0013] The level conversion of the signal level of latched indicative-data D is carried out to a voltage level (VDD-GND level) required for a liquid crystal drive by the next level-shifter circuit 1305 from a logic system voltage level (Vcc-GND level).

[0014] On the other hand, based on reference voltage VR (it constitutes from Vref1-Vref9), the reference voltage generating circuit 1309 is used for a gradation display by resistance division etc., for example, is generating the electrical potential difference of 64 level. The DA translation circuit 1306 is latched, and is changed and outputted to analog voltage based on indicative-data D (6 bits of each corresponding to DR, DG, and DB) by which the level conversion was carried out by choosing one voltage level from the electrical potential difference of 64 level of point **.

[0015] And this voltage level is outputted to the source signal line of each liquid crystal display component in a liquid crystal panel 901 from the liquid crystal driver voltage output terminal 1308 as a gradation display electrical potential difference by the output circuit 1307 constituted including the voltage follower circuit etc., respectively.

[0016] At such a conventional source driver, as shown in drawing 12 (only one circuit is indicated) and drawing 13, each is inputted serially (D1, D2, --D8 --), and the digital display data (DR, DG, DB) from the outside are once latched in the standup of clock signal CK by the input latch circuit 1301 which consists of D type flip-flops (DF/F is called hereafter) (see the timing chart of the latch data shown in drawing 14).

[0017] Then, each these-latched indicative-data D is inputted into the sampling memory circuit 1303 which consists of DF/F, it takes a synchronization in the standup of clock signal CK, takes a synchronization in the standup of the signal (SR1, SR2, --SRn) which is made to transmit the start pulse signal SP in n steps of shift register circuits 1302, and is outputted from each stage, and is memorized. Then, the output signal is held until each above-mentioned indicative-data D is outputted to the hold memory circuit 1304, then a package output is carried out from the hold memory

circuit 1304 by the latch signal LS and the following latch signal LS is inputted.

[0018]

[Problem(s) to be Solved by the Invention] However, in the above-mentioned conventional case, the following problems of degradation of display image quality of a liquid crystal panel 901 arise with highly-minute-izing more for improvement in display image quality. First, by the source driver 902 for carrying out in the case of the liquid crystal panel 901 of the SXGA (1024xRGBx768) mold using a total of 18 indicative-data D (6 bit xRGB) corresponding to RGB (for example, 64 gradation displays), a high-speed data transfer rate is very much needed [with 65MHz] in the above-mentioned former to the above-mentioned indicative-data D, for example.

[0019] Therefore, in the above-mentioned former, although it is necessary to memorize after a latch by the input latch circuit 1301, and to make the sampling memory circuit 1303 memorize indicative-data D by time sharing one by one with a quicker data transfer rate so that highly minute-ization of a liquid crystal panel 901 is aimed at, it becomes difficult to guarantee the specification (a data setup/hold time) of the timing which incorporates indicative-data D to clock signal CK by improvement in the speed.

[0020] In the above-mentioned former, display image quality deteriorated for the high data transfer rate, and the problem of it becoming impossible to fill the both sides of highly-minute-izing and improvement in display image quality to coincidence is produced from this.

[0021]

[Means for Solving the Problem] This invention is made in view of the above-mentioned conventional trouble. The purpose The method which incorporates indicative-data D with the standup of a clock signal and both the edges of falling is adopted as the input interface section so that a clock frequency can be reduced. By performing serial-parallel conversion inside a source driver, it is offering the semiconductor device expansion of clock frequency and whose dependability could reduce the clock frequency with the one half of a required data transfer rate, and improved, and the indicating-equipment module using it.

[0022] Namely, the semiconductor device of this invention is set to the semiconductor device which drives an indicating equipment based on an indicative-data signal, in order to solve the above technical problem. A transfer means to transmit the start pulse signal based on a clock signal, A latch means to incorporate the inputted indicative-data signal synchronizing with a clock signal, and to output as synchronous data, Based on the start pulse signal transmitted, it has a

sampling means to sample and output the above-mentioned synchronous data. The above-mentioned latch means It is characterized by synchronizing and incorporating the above-mentioned indicative-data signal to both the timing of the standup of the above-mentioned clock signal, and falling.

[0023] Said latch means may be equipped with the latch circuit of a two-piece unit for carrying out serial-parallel conversion of the indicative-data signal inputted serially in the above-mentioned semiconductor device.

[0024] As for said latch means, in the above-mentioned semiconductor device, it is desirable that it is what carries out serial-parallel conversion of the indicative-data signal inputted serially to both the timing of the standup of the plane 1 of said clock signal and falling.

[0025] According to the above-mentioned configuration, by outputting synchronous data for an indicative-data signal with a latch means synchronizing with a clock signal, and sampling and outputting the synchronous data with a sampling means based on the start pulse signal to which it was transmitted from the transfer means, the serial-parallel conversion of the above-mentioned indicative-data signal can be carried out, and it can change into a suitable signal to display with a display.

[0026] The specification (a data setup/hold time) of the timing which can reduce the data transfer rate of an indicative-data signal for the clock frequency of a clock signal more, and incorporates an indicative data to a clock signal can be made easy to guarantee, since a latch means moreover synchronized and incorporates the above-mentioned indicative-data signal in both the timing of the standup of the above-mentioned clock signal, and falling with the above-mentioned configuration.

[0027] In the semiconductor device which drives an indicating equipment based on an indicative-data signal in order that other semiconductor devices of this invention may solve the above technical problem A transfer means to transmit the start pulse signal based on a clock signal, A latch means to incorporate the inputted indicative-data signal synchronizing with a clock signal, and to output as synchronous data, Based on the start pulse signal transmitted, it has a sampling means to sample and output the above-mentioned synchronous data. The above-mentioned latch means It is characterized by synchronizing and incorporating the above-mentioned indicative-data signal to both the timing of each standup of two or more clock signals of each, with which phases differ mutually, and falling.

[0028] Said latch means may be equipped with the latch circuit of a four-piece unit for carrying out serial-parallel conversion of the indicative-data signal inputted serially in the above-mentioned semiconductor device.

[0029] As for two or more aforementioned clock signals of each, in the above-mentioned semiconductor device, it is desirable that the number of each above-mentioned clock signals is set up at the time of m (m is two or more integers) so that it may have the phase contrast of $1/(2m)$ mutually.

[0030] The specification (a data setup/hold time) of the timing which can reduce the clock frequency of a clock signal further from the required data transfer rate in an indicative-data signal, and incorporates an indicative data to a clock signal further can be made easier to guarantee, since a latch means synchronized and incorporates the above-mentioned indicative-data signal to both the timing of each standup of two or more clock signals of each, with which phases differ mutually, and falling according to the above-mentioned configuration.

[0031] In the above-mentioned semiconductor device, said display may be the liquid crystal display section. According to the above-mentioned configuration, since it can respond to highly minute-ization of the liquid crystal display section at stability,-izing of the improvement in the display image quality in a liquid crystal display can be carried out [certain].

[0032] The indicating-equipment module of this invention is characterized by having in the above any of each semiconductor device of a publication they are, in order to solve the above technical problem. According to the above-mentioned configuration, since it can respond to highly minute-ization in an indicating-equipment module at stability,-izing of the improvement in the display image quality of an indicating-equipment module can be carried out [certain].

[0033]

[Embodiment of the Invention] It will be as follows if each gestalt of operation of the indicating-equipment module using the semiconductor device and it concerning this invention is explained based on drawing 1 thru/or drawing 10 .

[0034] The liquid crystal display as the above-mentioned indicating-equipment module has the liquid crystal panel 1 of the TFT (thin film transistor) method which is the example of representation of an active matrix, and the liquid crystal driving gear (semiconductor device) for driving it as the liquid crystal display section, as shown in drawing 2 . About the detail of the above-mentioned liquid crystal panel 1, it mentions later.

[0035] The above-mentioned liquid crystal driving gear is equipped with the source driver 2 and gate driver 3 which consist of an IC, respectively, the controller 4, and the liquid crystal drive power source 5. A controller 4 is indicative-data D and a control signal S1 to the source driver 2. While outputting, in a gate driver 3, it is a control

signal S2. It outputs. The above-mentioned control signal S1 If it carries out, they are a Horizontal Synchronizing signal, a clock signal, and a control signal S2. If it carries out, a Vertical Synchronizing signal is mentioned.

[0036] And each liquid crystal driver voltage output terminal of the source driver 2 is connected to each corresponding source signal line 14 in a liquid crystal panel 1, and, on the other hand, each liquid crystal driver voltage output terminal of a gate driver 3 is connected to each corresponding gate signal Rhine 15 in a liquid crystal panel 1 (see drawing 3).

[0037] Moreover, the liquid crystal drive power source 5 is outputting the various driver voltages impressed to the power source which drives a liquid crystal driving gear (the source driver 2, gate driver 3), or a liquid crystal panel 1 to the liquid crystal driving gear.

[0038] The source driver 2 and gate driver 3 of the above-mentioned liquid crystal driving gear are each TCP (Tape Carrier Package) which is not illustrated, for example. It is carried. TCP means the thin package which equipped the tape film with LSI.

[0039] As opposed to the terminal (it connects with the source signal line 14 of point **, or gate signal Rhine 15) which consists of ITO (Indium Tin Oxide: indium tin oxide) prepared on the liquid crystal glass substrate which a liquid crystal panel 1 does not illustrate, through ACF (Anisotropic Conductive Film: anisotropy electric conduction film), thermocompression bonding of the output terminal side of TCP is carried out, and it is connected electrically.

[0040] On the other hand, I/O of the input-side signal to each source driver 2 and a gate driver 3 is performed through TCP wiring, flexible substrate wiring, etc. The serial digital display data inputted from the outside let a controller 4 pass, and are inputted into the source driver 2 as serial indicative-data D.

[0041] An example of the circuit block diagram in the above-mentioned source driver 2 as a gestalt of operation of the first of this invention is shown in drawing 1 . The source driver 2 has the output terminal 28 and the reference voltage generating circuit 29 from a shift register circuit (transfer means) 22, the input latch circuit (latch means) 21, the sampling memory circuit (sampling means) 23, the hold memory circuit 24, the level-shifter circuit 25, the DA translation circuit 26, an output circuit 27, and an output circuit 27 fundamentally. Only difference with the conventional technique is first explained among the above-mentioned circuitry below, and the explanation about other circuit actuation is mentioned later.

[0042] As the former showed difference to drawing 12 and drawing 13 , the input latch circuit 1301 which is incorporation and transfer of indicative-data D centering on the

input latch circuit 1301 and the sampling memory circuit 1303 which latch inputted indicative-data D, and consisted of one DF/F for every bit of indicative-data D (DR, DG, DB respectively 6 bits and a total of 18 bits configuration) of a digital type was installed.

[0043] This invention performs the latch of indicative-data D in the input latch circuit 21 using both the edges of the standup of clock signal CK, and falling, is *****, and is reduction, i.e., the thing made quickly (a data transfer rate is improved), from the former about the processing speed of indicative-data D in future circuits to the clock frequency of clock signal CK.

[0044] The gestalt of operation of the first of this invention is explained based on the example of a circuit of drawing 4 , and the timing chart of drawing 5 . First, to 1 bit each of serial indicative-data D (DR, DG, DB respectively 6 bits and a total of 18 bits configuration) outputted from a controller 4, the input latch circuit 21 is synchronized with both the edges of the standup of clock signal CK, and falling, is incorporated, and is outputted as each synchronous data Q11 and Q12, respectively.

[0045] For this reason, the above-mentioned input latch circuit 21 has two DF/F of DF/F21b into which DF/F21a into which indicative-data D and clock signal CK are inputted, respectively, and the above-mentioned indicative-data D and the reversal clock signal CK bar which reversed above-mentioned clock signal CK by inverter 21i are inputted, respectively. While the above-mentioned indicative-data D is inputted into D terminals each of DF/F21a, and DF/F21b, clock signal CK and a reversal clock signal CK bar are inputted into each CK terminal of DF/F21a and DF/F21b, respectively.

[0046] Two DF/F 23a1 for inputting each two synchronous data Q11 and Q12 outputted from the input latch circuit 21, respectively, and making them latch to the sampling memory circuit 23 DF/F 23b1 It is installed.

[0047] And DF/F 23a1 which starts and inputs the synchronous data Q11 In CK terminal, it is A (1) of a shift register circuit 22. DF/F 23b1 into which the output of eye a stage, on the other hand, inputs the falling synchronous data Q12 In CK terminal, it is B (1) of a shift register circuit 22. The output of eye a stage is inputted.

[0048] Incidentally, n steps of shift register circuits 22 are A (1) which takes a synchronization in the standup of clock signal CK, and transmits the start pulse signal SP one by one. A (2) -- A (n/2) B which takes a synchronization in the shift register section and falling of clock signal CK, and transmits the start pulse signal SP one by one (1) B (2) -- B (n/2) It has the shift register section.

[0049] Each output (Q21, Q22) of the sampling memory circuit 23 is inputted into the

predetermined address of the hold memory circuit 24, respectively, and is memorized. The circuit shown in drawing 4 is a circuit for 1 bit (as DR1) of each indicative datas DR, DG, and DB in indicative-data D of a total of 18 bits, and is eye A (1) stage of a shift register circuit 22, and B (1) further. Only the part sampled to the timing of eye a stage is illustrated as an example of representation.

[0050] although not illustrated -- indicative data DR1 the output Q11 of the inputted input latch circuit 21 -- other A (2) of a shift register circuit 22 --A (n/2) the output of eye a stage can be set to the sampling memory circuit 23 inputted into CK terminal, respectively -- each -- $DF/F23a2 - DF/F23an / 2$ It is inputted in common. Each output of these sampling memory circuit 23 is inputted into the predetermined address of the hold memory circuit 24, respectively, and is memorized.

[0051] on the other hand -- indicative data DR1 the output Q12 of the inputted input latch circuit 21 -- other B (2) of a shift register circuit 22 --B (n/2) the output of eye a stage can be set to the sampling memory circuit 23 inputted into CK terminal, respectively -- each -- it is inputted common to $DF/Fb2 - DF/Fbn/2$. Each output of these sampling memory circuit 23 is inputted into the predetermined address of the hold memory circuit 24, respectively, and is memorized.

[0052] The above is an indicative data DR1. Although it is the circuitry and the example of processing which are related, it has circuitry similarly processed to other indicative datas in indicative-data D, and is processed similarly. Thus, it means that serial-parallel conversion of the above-mentioned indicative-data D was carried out.

[0053] The various timing charts of above-mentioned clock signal CK and indicative-data D are shown in drawing 5 . Reference] is latched [drawing 5 / indicative-data D[/ which was inputted / (b)] with both the edges of the standup and falling of reference] in clock signal CK[drawing 5 (a), and falling latch data [drawing 5 (d) which is reference] and the falling synchronous data Q12 about standup latch data [drawing 5 (c) which is the standup synchronous data Q11 is divided into two channels of reference].

[0054] Therefore, serial-parallel conversion of said indicative-data D will be carried out per two pieces. That is, two parallel data with which the data length doubled in 1 time of a conversion cycle are generated. here -- it should observe -- the clock frequency of clock signal CK is good in the one half of the data transfer rate of indicative-data D, and if a data transfer rate is 80MHz, a clock frequency is good at 40MHz.

[0055] Thus, by this invention, a clock frequency can realize the liquid crystal display module using a liquid crystal driving gear (semiconductor device) and it with high

expansion of clock frequency called one half of the data transfer rate of indicative-data D and dependability by incorporation of indicative-data D with the standup of clock signal CK and both the edges of falling, and adopting mode of processing.

[0056] Next, it will be as follows if the gestalt of the second operation as a gestalt of other operations concerning this invention is explained based on drawing 6 thru/or drawing 8 .

[0057] In the gestalt of said first operation, it was considering as the configuration into which clock signal CK of a plane 1 is inputted from a controller 4. In this case, by the method which it memorizes after a latch by said input latch circuit 21, and makes the sampling memory circuit 23 memorize indicative-data D of a quicker data transfer rate accompanying highly-minute-izing by time sharing one by one further, it may become difficult to clock signal CK to guarantee the specification (a data setup/hold time) of data incorporation timing.

[0058] so, in the liquid crystal driving gear as a semiconductor device in the gestalt of this second operation Each clock signal CK1 of two phases which carried out [1 / / 4 ****] the phase as shown in drawing 6 thru/or drawing 8 , CK2 Use and the incorporation method of indicative-data D with both the edges of a standup and falling by adopting it as the input latch circuit 31 and a list at the shift register circuit 32 and the sampling memory circuit 33 as a processing circuit A clock frequency is made to one fourth of the required data transfer rates in indicative-data D, and the liquid crystal display module using expansion of clock frequency, a reliable liquid crystal driving gear (semiconductor device), and this liquid crystal driving gear can be realized further.

[0059] The circuitry Fig. of the source driver 2 which starts the gestalt of operation of **** 2 at drawing 7 is shown. The main differences with the source driver 2 shown by drawing 1 are each clock signal CK1 of two phases, and CK2 at the gestalt of this second operation to clock signal CK of a plane 1 being inputted into the input latch circuit 21 for latching indicative-data D with the gestalt of the first operation. It is the point of being inputted into the input latch circuit 31, respectively.

[0060] Below, the above-mentioned input latch circuit 31, the sampling memory circuit 33, and a shift register circuit 32 are explained. Since it is the same as that of the gestalt of the first operation of the above-mentioned about the configuration and actuation about the hold memory circuit 24, the level-shifter circuit 25, the DA translation circuit 26, an output circuit 27, and the reference voltage generating circuit 29, the same member number is given and those explanation is omitted below.

[0061] To drawing 7 , the timing chart is illustrated for the example of a circuit of the input latch circuit 31 concerning this invention, the sampling memory circuit 33, and a shift register circuit 32 at drawing 8 . Clock signal CK1 which acted [1 / / 4 ****] as the latch of indicative-data D in the input latch circuit 31 the phase mutually with the gestalt of the second operation And clock signal CK2 It uses and they are each clock signal CK1 of both and CK2. The processing speed of the above-mentioned indicative-data D in future circuits can be further reduced by latching indicative-data D, using both the edges of a standup and falling respectively.

[0062] If the gestalt of implementation of the above second is explained in more detail based on drawing 7 and drawing 8 , the input latch circuit 31 has first four DF/F inputted into D terminal whose above-mentioned indicative-data D is an input terminal, respectively to 1 bit each of indicative-data D (DR, DG, DB respectively 6 bits and a total of 18 bits configuration) outputted from a controller 4. Four above-mentioned DF/F is DF/F31a and clock signal CK1. Reversal clock CK 1 reversed in inverter 31i It is [DF/F31b which used the bar, and] clock signal CK1 further. Clock signal CK2 which received and carried out [1 / / 4 ****] the phase They are two DF/F31c and DF/F31d which is constituted like the point and operates.

[0063] The sampling memory circuit 33 is four DF/F 33a1 for inputting four outputs (Q11, Q12, Q13, Q14) from the input latch circuit 31, respectively, and making them latch, DF/F 33b1, DF/F 33c1, and DF/F33d1. It is installed.

[0064] And DF/F 33a1 which starts and inputs the synchronous data Q11 into D terminal In CK terminal, it is A (1) of a shift register circuit 32. DF/F25b1 as which the output of eye a stage, on the other hand, inputs the falling synchronous data Q12 into D terminal In CK terminal, it is B (1) of a shift register circuit 32. The output of eye a stage is inputted.

[0065] DF/F 33c1 which inputs 1 / 4 phase-shift ***** synchronous data Q13 into a pan at D terminal In CK terminal, it is C (1) of a shift register circuit 32. DF/F33d1 as which the output of eye a stage, on the other hand, inputs the falling synchronous data Q14 into D terminal In CK terminal, it is D (1) of a shift register circuit 32. The output of eye a stage is inputted.

[0066] Incidentally n steps of shift register circuits 32 Clock signal CK1 A which takes a synchronization in a standup and transmits the start pulse signal SP one by one (1) A (2) -- A (n/4) Shift register section, Clock signal CK1 B which takes a synchronization in falling and transmits the start pulse signal SP one by one (1) B (2) -- B (n/4) Shift register section, Furthermore, it is clock signal CK2. C which takes a synchronization in a standup and transmits the start pulse signal SP one by one (1) C

(2) -- C (n/4) Shift register section, Clock signal CK2 D which takes a synchronization in falling and transmits the start pulse signal SP one by one (1) D (2) -- D (n/4) It has the shift register section.

[0067] Each output (Q21, Q22, Q23, Q24) of the sampling memory circuit 33 is inputted into the predetermined address of the hold memory circuit 24, respectively, and is memorized. The circuit of drawing 6 is a circuit of the sake for 1 bit (as DR1) of a total of 18 bits of each indicative datas DR, DG, and DB in indicative-data D, and is A (1) of a shift register circuit 32 further. Eye a stage and B (1) Eye a stage and C (1) Eye a stage and D (1) Only the part sampled to the timing of eye a stage is illustrated as an example of representation.

[0068] Although not illustrated, it is an indicative data DR1. The synchronous data Q11 which are the output of the inputted input latch circuit 31 are other A (2) of a shift register circuit 32. --A (n/4) DF/F33a2 --DF/D33an/4 which inputs the output of eye a stage into CK terminal, respectively It is inputted common to D terminal, respectively. And the output of these sampling memory circuit 33 is inputted into the predetermined address of the hold memory circuit 24, respectively, and is memorized.

[0069] On the other hand, it is an indicative data DR1. The synchronous data Q12 which are the output of the inputted input latch circuit 31 are other B (2) of a shift register circuit 32. --B (n/4) DF/F33b2 --DF/D33bn/4 which inputs the output of eye a stage into CK terminal, respectively and which is not illustrated It is inputted common to D terminal, respectively. And the output of these sampling memory circuit 33 is inputted into the predetermined address of the hold memory circuit 24, respectively, and is memorized.

[0070] Hereafter, also about each synchronous data Q13 and Q14 which are each output of the input latch circuit 31, the same actuation as previous explanation is carried out, and outputs Q23 and Q24 are outputted to the following hold memory circuit 24, and are memorized. The above is an indicative data DR1. Although it is a circuit, they are a configuration with other same indicative datas in indicative-data D, and processing.

[0071] Therefore, with the gestalt of the second operation, serial-parallel conversion of said indicative-data D will be carried out per four pieces. That is, four parallel data with which the data length increased 4 times are generated in 1 time of a conversion cycle. here -- it should observe -- it is that a clock frequency can use the thing of the quarter (1/4) of indicative-data D, and if the data transfer rate of the above-mentioned indicative-data D is 80MHz, the above-mentioned clock frequency is good at 20MHz.

[0072] Thus, each clock signal CK1 which set up the phase so that it might differ mutually and CK2 By the standup and adopting the incorporation method and processing circuit of indicative-data D with both the edges of falling, since the data transfer rate of a clock frequency and indicative-data D can be set to one fourth, the liquid crystal display module using a liquid crystal driving gear and it with still higher correspondence to expansion of clock frequency and dependability is realizable.

[0073] At the gestalt of implementation of the above second, they are clock signal CK1 of two phases, and CK2. Although the used example explained, they are each clock signals CK1-CKm of m phase. It is also possible to use, and to latch and process indicative-data D. In $m=2k$ ($k=0, 1, 2$ and $3, \dots$), the circuitry following a degree has especially good adjustment. In this case, m clock signals CK1-CKm What is necessary is just to shift a phase a $1/(2m)$ phase every mutually one by one.

[0074] As mentioned above, although this invention has been explained using a liquid crystal driving gear This invention was called not only a liquid crystal driving gear but above-mentioned source driver 2. Carry out cascade connection of one piece or two or more semiconductor devices for a display device drive, and the start pulse signal SP is synchronously transmitted by clock signal CK. It is effective to the display which incorporates indicative-data D with this transfer signal, displays by applying a latch a certain period, and displays one screen by repeating this.

[0075] Especially this invention was called the above-mentioned source driver 2 and an above-mentioned gate driver 3. Provide a driving gear in the direction of X, and the direction of Y, and said start pulse signal SP is transmitted to them synchronizing with clock signal CK. It is effective in big-screen-izing of the display screen of the indicating equipment which chooses a video signal as time sharing with this transfer signal, incorporates, displays by applying a latch a Horizontal Synchronizing signal period, repeats this and displays one screen, and high-reliability-izing of the fast transfer of the indicative data accompanying highly-minute-izing.

[0076] Moreover, by the ability of the clock frequency of clock signal CK inside a semiconductor device to be reduced, it can respond also to a low-battery drive and low-power-ization also becomes possible as a result. Furthermore, a reliable semiconductor device is realizable also from low noise-ization by clock frequency reduction.

[0077] Moreover, with each gestalt of the above-mentioned operation, although the configuration which mounted the semiconductor device which carried the chip of source driver 2 grade in TCP by thermocompression bonding through the anisotropy electric conduction film (ACF) etc. as opposed to the electrode (ITO line) of a liquid

crystal panel 1 explained, this invention may be carried also including a controller 4 on included insulating tapes, such as a flexible substrate, a film, etc. instead of a TCP gestalt.

[0078] Furthermore, the configuration of having mounted the semiconductor device in the electrode (ITO line) of a liquid crystal panel 1 directly by thermocompression bonding for example, through the anisotropy electric conduction film (ACF) etc. with the chip gestalt as a chip-on glass (COG) method is sufficient as this invention, and the circuit in glass (CIG) method which formed the circuit on the glass substrate of a liquid crystal panel 1 with the low-temperature polish recon technique etc. further can also realize it.

[0079] Next, the configuration and actuation of said liquid crystal panel 1 are explained below based on drawing 3 , drawing 9 , and drawing 10 . As shown in a liquid crystal panel 1 at drawing 3 , the counterelectrode 6 which meets through the liquid crystal which is not illustrated is formed to gate signal Rhine 15 for driving the source signal line 14 for driving TFT13 and the above TFT13 as a switching element which turns on and off the electrical-potential-difference impression to the pixel electrode 11, the pixel capacity 12, and the pixel electrode 11, and the above TFT13, and the pixel electrode 11. In the above-mentioned liquid crystal panel 1, the pixel capacity 12 is formed between each pixel electrode 11 and a counterelectrode 6 through the liquid crystal which is not illustrated, respectively.

[0080] The field shown by A is a liquid crystal display component for 1 pixel among drawing 3 . The gradation display electrical potential difference of 64 gradation is given to the source signal line 14 from the source driver 2 shown in drawing 2 , having corresponded to the brightness of the pixel for a display. A scan signal is given to each gate of TFT13 so that TFT13 located in a line with the lengthwise direction may carry out sequential ON from a gate driver 3 in gate signal Rhine 15.

[0081] It lets TFT13 of an ON state pass, the electrical potential difference of the source signal line 14 is impressed to the pixel electrode 11 connected to the drain of the above TFT13, a charge is accumulated in the pixel capacity 12 between counterelectrodes 6, and when the light transmittance of liquid crystal changes according to the amount of charges, the gradation display by each pixel is performed.

[0082] An example of a drive wave to the liquid crystal display component and pixel in the time of a gradation display which is different in drawing 9 and drawing 10 (for example, the example of a white display and the example of a black display) is shown. it is shown in drawing 9 and drawing 10 -- as -- a drive wave -- 51 and a drive wave -- the drive wave by which 41 was outputted to the source signal line 14 from the

liquid crystal driver voltage output terminal of the source driver 2, respectively -- on the other hand -- a drive wave -- 52 and a drive wave -- 42 is the drive wave outputted to gate signal Rhine 15 from the liquid crystal drive output terminal of a gate driver 3, respectively.

[0083] Moreover, potential 53 and potential 43 are the potentials of a counterelectrode 6, and applied voltage 54 and applied voltage 44 are voltage waveforms impressed to the pixel electrode 11. Therefore, the electrical potential difference impressed to liquid crystal is the electrical-potential-difference difference of the pixel electrode 11 and a counterelectrode 6, and is shown by the height of a slash field all over drawing.

[0084] drawing 9 -- the drive wave from the liquid crystal driver voltage output terminal of a gate driver 3 -- the time of 52 being High level -- TFT13 -- turning on -- the drive wave from the liquid crystal driver voltage output terminal of the source driver 2 -- the potential difference of 51 and the potential 53 of a counterelectrode 6 is impressed to the pixel electrode 11. then, the drive wave from the liquid crystal driver voltage output terminal of a gate driver 3 -- 52 -- Low It will be set to level and TFT13 will be in an OFF state. Since it has the pixel capacity 12 by each pixel, respectively at this time, above-mentioned applied voltage is held.

[0085] The same is said of the case of drawing 10 . The electrical potential difference impressed to the liquid crystal which constitutes a pixel is different, and drawing 9 and drawing 10 have high applied voltage 54 compared with the applied voltage 44 in the case of drawing 10 , when it is drawing 9 . Thus, by changing the electrical potential difference impressed to liquid crystal as analog voltage, the light transmittance of liquid crystal was changed in analog, and the multi-tone display by each pixel is realized. The number of gradation which can be displayed is determined by the number of the alternative of the analog voltage impressed to liquid crystal.

[0086] Next, it is inputted into the hold memory circuit 24, and the memorized processing after receiving indicative-data D by which parallel conversion was carried out is explained below based on drawing 1 and drawing 3 .

[0087] First, when the data of 1 level period of this indicative-data D are inputted into the hold memory circuit 24, it is latched by the latch signal LS based on a Horizontal Synchronizing signal. And during 1 level period, previous indicative-data D is held and is outputted from the hold memory circuit 24 until the following latch signal LS is inputted that is,.

[0088] The level conversion of the signal level of latched indicative-data D is carried out to a voltage level (VDD-GND level) required for a liquid crystal drive by the next

level-shifter circuit 25 from a logic system voltage level (V_{cc} -GND level).

[0089] On the other hand, based on reference voltage VR (it constitutes from V_{ref1} - V_{ref9}), the reference voltage generating circuit 29 is used for a gradation display by resistance division etc., for example, is generating the electrical potential difference of 64 level. The DA translation circuit 26 is latched, and is changed and outputted to analog voltage based on indicative-data D (6 bits of each corresponding to DR, DG, and DB) by which the level conversion was carried out by choosing one voltage level from the electrical potential difference of 64 level of point **.

[0090] And this voltage level is outputted to the source signal line 14 of each liquid crystal display component in a liquid crystal panel 1 from the liquid crystal driver voltage output terminal 28 as a gradation display electrical potential difference by the output circuit 27 constituted including the voltage follower circuit etc., respectively, and the gradation display based on indicative-data D is made.

[0091] By the way, in the former, when the clock frequency of clock signal CK is highly set up corresponding to having set up the data transfer rate of indicative-data D highly for highly-minute-izing of a display image, since it becomes difficult to secure the duty ratio (yes, ratio of a period and a low period) of clock signal CK inside the source driver 902, there is a possibility of causing reduction of the clock frequency of clock signal CK. For this reason, in the above-mentioned former, since it becomes unstable to carry out serial-parallel conversion of the indicative-data D by reduction of clock frequency, it has the problem that degradation of display image quality may be invited.

[0092] However, in this invention, since the clock frequency of clock signal CK can be low set up even if it sets up the data transfer rate of indicative-data D highly for highly-minute-izing of a display image, the above-mentioned problem is avoidable.

[0093]

[Effect of the Invention] A transfer means by which the semiconductor device of this invention transmits the start pulse signal based on a clock signal as mentioned above, A latch means to incorporate the inputted indicative-data signal synchronizing with a clock signal, and to output as synchronous data, Based on the start pulse signal transmitted, it has a sampling means to sample and output the above-mentioned synchronous data. The above-mentioned latch means It is the configuration of synchronizing and incorporating the above-mentioned indicative-data signal to both the timing of the standup of the above-mentioned clock signal, and falling.

[0094] So, while being able to carry out serial-parallel conversion for a display, the above-mentioned configuration an indicative-data signal Since a latch means

synchronizes and incorporates the above-mentioned indicative-data signal to both the timing of the standup of the above-mentioned clock signal, and falling. Since the specification (a data setup/hold time) of the timing which can reduce the clock frequency of a clock signal from the data transfer rate of an indicative-data signal, and incorporates an indicative data to a clock signal can be made easy to guarantee, The effectiveness that the both sides of highly-minute-izing and improvement in display image quality can be filled to coincidence is done so, avoiding degradation of display image quality.

[0095] A transfer means by which other semiconductor devices of this invention transmit the start pulse signal based on a clock signal as mentioned above, A latch means to incorporate the inputted indicative-data signal synchronizing with a clock signal, and to output as synchronous data, Based on the start pulse signal transmitted, it has a sampling means to sample and output the above-mentioned synchronous data. The above-mentioned latch means It is the configuration of synchronizing and incorporating the above-mentioned indicative-data signal to both the timing of each standup of two or more clock signals of each, with which phases differ mutually, and falling.

[0096] So, since the above-mentioned configuration synchronizes and incorporates the above-mentioned indicative-data signal to both the timing of each standup of two or more clock signals of each, with which phases differ mutually, and falling, a latch means Furthermore, the clock frequency of a clock signal can be reduced from the data transfer rate of an indicative-data signal. The effectiveness that the both sides of highly-minute-izing and improvement in display image quality can be filled to coincidence is done so, avoiding degradation of display image quality, since the specification (a data setup/hold time) of the timing which incorporates an indicative data to a clock signal can be made easier to guarantee.

[0097] The indicating-equipment module of this invention is characterized by having any of the above-mentioned semiconductor device they are as mentioned above. According to the above-mentioned configuration, since it can respond to highly minute-ization in an indicating-equipment module, the effectiveness that-izing of the improvement in the display image quality of an indicating-equipment module can be carried out [certain] is done so.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of a source driver concerning this invention for driving the liquid crystal display as an indicating-equipment module of this invention showing the gestalt of the first operation.

[Drawing 2] It is the block diagram showing the above-mentioned liquid crystal display.

[Drawing 3] It is the outline block diagram of the liquid crystal panel in the above-mentioned liquid crystal display.

[Drawing 4] It is the important section block diagram of the above-mentioned source driver.

[Drawing 5] It is the timing chart which shows incorporation actuation of indicative-data D of the above-mentioned source driver.

[Drawing 6] It is the block diagram of a source driver concerning this invention showing the gestalt of the second operation.

[Drawing 7] It is the important section block diagram of the above-mentioned source driver.

[Drawing 8] It is the timing chart which shows incorporation actuation of indicative-data D of the above-mentioned source driver.

[Drawing 9] It is the timing chart which shows actuation of the above-mentioned liquid crystal panel.

[Drawing 10] It is the timing chart which shows other actuation of the above-mentioned liquid crystal panel.

[Drawing 11] It is the block diagram of the conventional liquid crystal display.

[Drawing 12] It is the block diagram of a source driver used for the above-mentioned liquid crystal display.

[Drawing 13] It is the important section block diagram of the above-mentioned source driver.

[Drawing 14] It is the timing chart which shows actuation of the above-mentioned source driver.

[Description of Notations]

21 Input Latch Circuit (Latch Means)

22 Shift Register Circuit (Transfer Means)

23 Sampling Memory Circuit (Sampling Means)